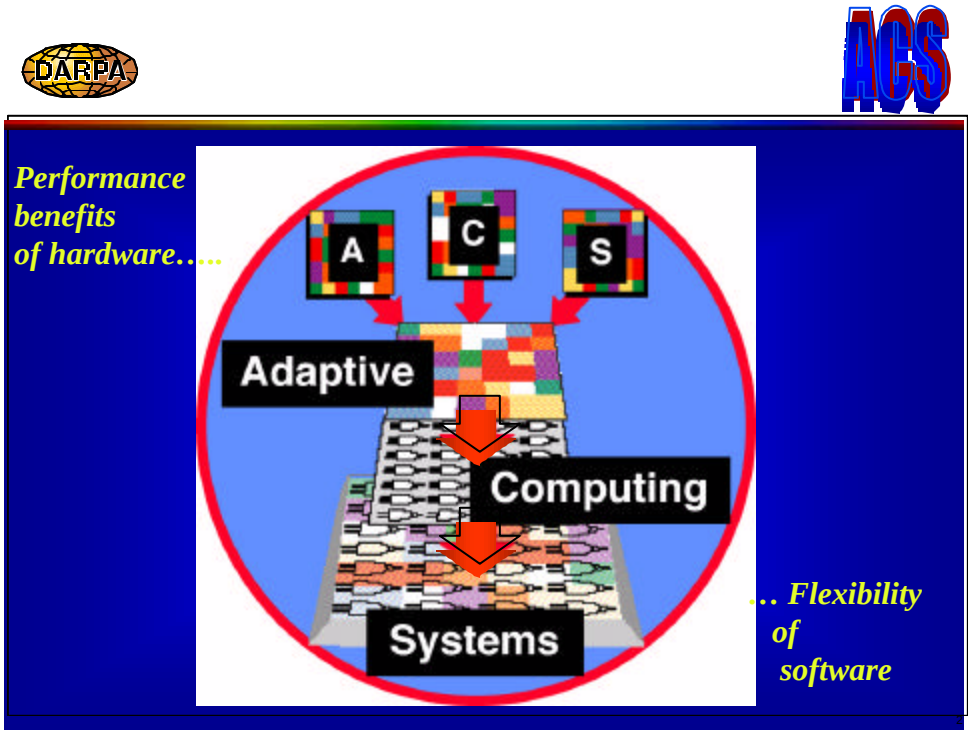
ACS Program Overview

First NASA/DoD Workshop on Evolvable Hardware

July 19 - 21, 1999



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Program Concept

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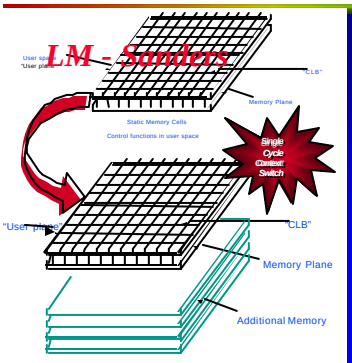
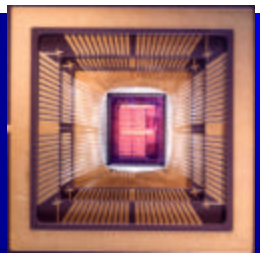
Context Switchable Reconfigurable Computer





World's First!!

Dynamically Reconfigurable (logic function implementations changed while processing is underway)

Multiple (multiple contexts stored internally on device)

Context Switching (replacing one logic function implementation in an FPGA with another) *Device* (multiple contexts and FPGA within single device)

CSRC Effort:

- Optimized for DSP *and* Glue Logic
- Capable of internally storing 4 contexts
- Contexts can be switched in *ONE* clock cycle
  - Data in flip-flops & LUTS can be shared between contexts
  - Two data sharing schemes (*global* and *public/private addressable*)
  - Context switch initiated either by internal logic *or* by external pins
  - Background loading of contexts

First CSRC Prototype Device Has Been Produced

Actel Introduces New Line

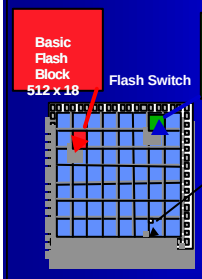
Modular ProASIC Architecture
Combines SRAM, FLASH, and Logic Cells
Providing a Very High Density FPGA for Configurable Computing

Research funded by ACS program to Zycad/Gatefield

- Utilize FLASH memory within FPGA architecture

Chip Area	1/4 SRAM
Metal Capacitance	1/2 SRAM
Speed	1.5 ~ 2x SRAM
Power	1/2 SRAM

- The FLASH-based FPGAapproach provides devices that are uniquely non-volatile and reprogrammable
- Optimized tile and routing architecture to improve gate utilization and device performance
- Achieved a 10x Speed Improvement with ASICMaster Place & Route software
- Developed GF260F180 architecture with embedded memory providing 180K gates of reconfigurable logic
- *Signed agreement with Siemens for 0.25 technology to support fabrication of devices approaching 500K gates - June 1998*
- *Formed Strategic Alliance between Actel and Gatefield - August 1998*



Successful transition into a larger market segment by a major market leader

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ACS Insertion

DARPA Geolocation effort using GateField Modular ProASIC Architecture FPGA to implement LORAN

- Replaces a PC and TMS320C30 DSP card solution with a single FPGA, single PC/104 board solution . . . removed need for any "glue logic"
- The LORAN implementation was used in the Geolocation demonstration in November 1998 at Fort Benning's military operations in urban terrain facility
- Resulted in a single board solution that was *impossible* without going to a costly and time consuming ASIC implementation

FPGA solution can be altered to address future/changed requirements

PC + DSP board

Single 3.75 x 3.55 inch PC/104 card implementation

GATEFIELD

Commercial ACS Board Product

Annapolis Micro Systems

Completed Fall 1998

WASPP

NEW IDEAS

- Hybrid FPGA/DSP co-processor architecture
- Design methodology for FPGA/DSP co-design
- Automatic target recognition (ATR) image processing kernels using hybrid FPGA/DSP architecture

FUTURE

- Continued Involvement in ACS community
- Evolution of new commercial products within ACS community and ACS applications

IMPACT

- Formal design methodology greatly improves productivity of application designers using hybrid FPGA/DSP systems
- High-performance ATR system development made easier and better

New AMS board supporting new Xilinx Virtex chip significantly influenced by DARPA ACS SLAAC!!

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ACS ARCHITECTURE EFFORTS already IMPACT COMMERCIAL RECONFIGURABLE PRODUCTS

ACS RISC + Reconfigurable Array architectures entering commercial products

Triscend

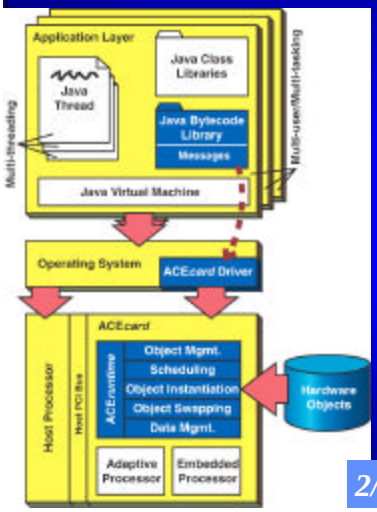
- Trisend (http://www.triscendcorp.com/) announces industry's first 32-bit configurable processor family
  - SRAM-based configurable system logic cells
  - ARM7TDMI™ RISC core
  - agreement with SHARP to produce devices in 1999
- Chameleon Systems (http://www.cmln.com/)
  - combining flexibility of FPGAs, performance of dedicated custom silicon, and programmability of microprocessors
- Adaptive Silicon Inc., new company spin-off from National Semi-Conductor looking to produce "NAPA-1000"

Berkeley BRASS effort

Commercial ACS Java Products

GOAL

To develop the enabling technologies that allow adaptive hardware to be easily utilized by application developers



NEW IDEAS

- Java bytecode, atomic and hardware objects
- Adaptive computing class library and API
- Automatic composition of library elements
  - during application development
  - during execution
- Multi-threaded, multi-user execution environment for adaptive computing
- Scheduling, instantiation and communication of functional elements
- Java-based application design

Two Primary Areas of Development

- ***Application Design (Abstractions)***
- ***Execution Environment (Infrastructure)***

ACS meets Java

DEVELOPING

- Hardware objects
- Application design environments
- Execution environments

IMPACT

- Faster implementation of ACS designs
- Accelerate general purpose computing
- 10 X increase in user productivity - reduced algorithm development and mapping time

Developed FPGA Card, available as commercial product, will use for demonstrations

ACE2

2/3Qtr FY99 Demonstration

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ACS Architecture Efforts already Impact Commercial Reconfigurable Products

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Berkeley BRASS effort

ACS Challenge Problems

- **Surveillance Challenge Problem (Sandia National Lab)**
- **IR Automatic Target Recognition: Tank Application (Night Vision Lab)**
- **Sonar Adaptive Beamforming (Naval Undersea Warfare Center)**
- **INFOSEC Separation Challenge (National Security Agency)**
- **INFOSEC Architectures for Security (NSA)**
- **Video: Face Recognition (NSA)**
- **Video: Text Recognition (NSA)**
- **Fault-tolerant/Low-power Applications (JPL)**
- **RF Transient Signal Analysis (Los Alamos National Lab)**
- **Plume Detection and Laser Spectral Analysis (LANL)**

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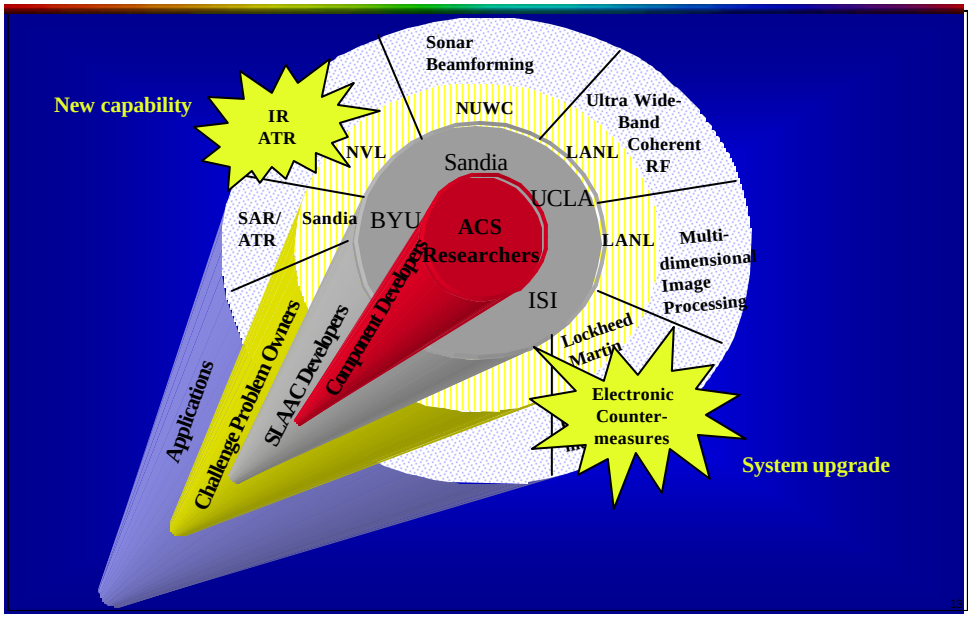
Near-Term Demos

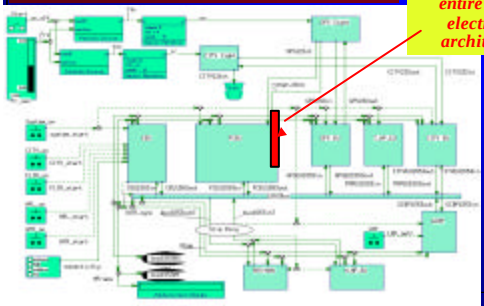


Near Term Insertions/Demo

ARMY NIGHT VISION LABORATORY - IR/ATR

Insert ATR capability into existing M1A2 Architecture

M1A2 Top Level Architecture



ATR allowed 2 VME slots within entire M1A2 electronics architecture

Utilize ACS/EHPC Technology to enable IR/ATR Processor

Approach

Demonstration of ATR cueing for the M1A2 tank ATR mission utilizing ACS/Embedded technologies.

Utilize processor testbed with mature ATR algorithms for processing of 2nd GEN FLIR image data.

Work with PM-Abrams/TACOM/TARDEC & PM Night Vision on technology insertion plan.

Impact

- First demonstration of Army ATR cueing mission within physical requirements
- Enable 10 Hz ATR frame rate
- Addresses robustness of processor technology for future changes.
- Path to retrofit current fielded & integrate within future Army ground platforms

3Qtr FY99 Demonstration

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NVL IR/ATR Demonstration

- System
  - Target cues (det not rec/ID) on operator's display
  - 1315 x 480 x 12 bit 2nd Gen FLIR data input
  - 10 Hz update rate
  - Latency: 100 ms
  - Programmable
- Physical
  - 2 6U sized board slots
  - < 100 Watts
  - No impact on existing tank electronics

Only the ACS/EHPC solution is capable of meeting the 10 Hz and latency requirement, within the physical constraints, while also providing future algorithm flexibility!!

Current NVL ATR Processing Performance Estimates

(ATR is composed of five processing levels, with the first round the most processing intensive)

Round (time in sec.)	Sun Ultra-60 300 MHz (optimized)	Mercury (single G3 PPC Bd.) 300 MHz (optimized code)	CSPI (quad 603e PPC Bd.) 200 MHz (non-optimized code)	ACS/CSPI (ACS tri- Virtex 1000 Bd.) 100 MHz (quad G3 PPC Bd.) 400 MHz	
0	8.53	9.22	3.12	0.06	ACS
1	0.37	0.12	0.18	0.015	
2	0.27	0.20	0.28	0.010	
3	0.11	0.10	0.16	0.005	EHPC
4	0.03	0.025	0.06	0.001	
Total	9.31	9.67	3.80	0.091	100X!!

Near Term Insertion/Demo

Electronic Countermeasures Analysis (ECMA) Insertion

AN/SPY-1 GSA CABINET (4 BAY)

Lockheed-Martin

- ***Current AN/SPY-1 Radar ECMA Equipment Was Designed in the 1970s***
  - Module Functions Hard-Wired
  - Modification is Difficult;Impacts Ship Schedules
  - Current Subsystem Cannot Adapt to New Threats
  - ECMA Processor Consumes Entire Equipment Frame
- ***Current Shipboard ECMA Processor Requires Upgrade***
  - Current ECMA frame is completely full, no room for growth
  - AEGIS MUST respond to new TBMD mission;
  - Must be able to respond to new threat scenarios

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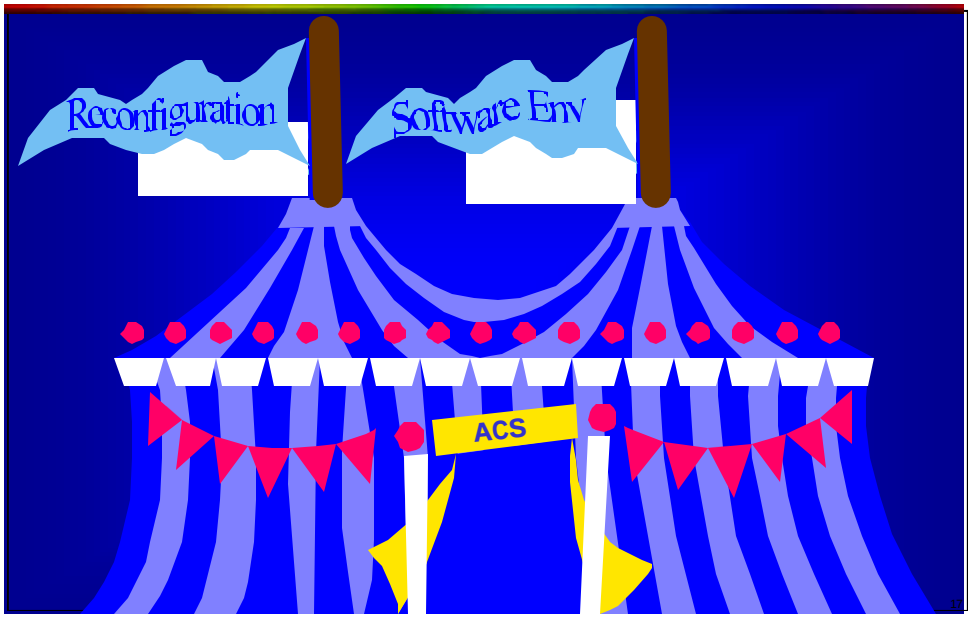
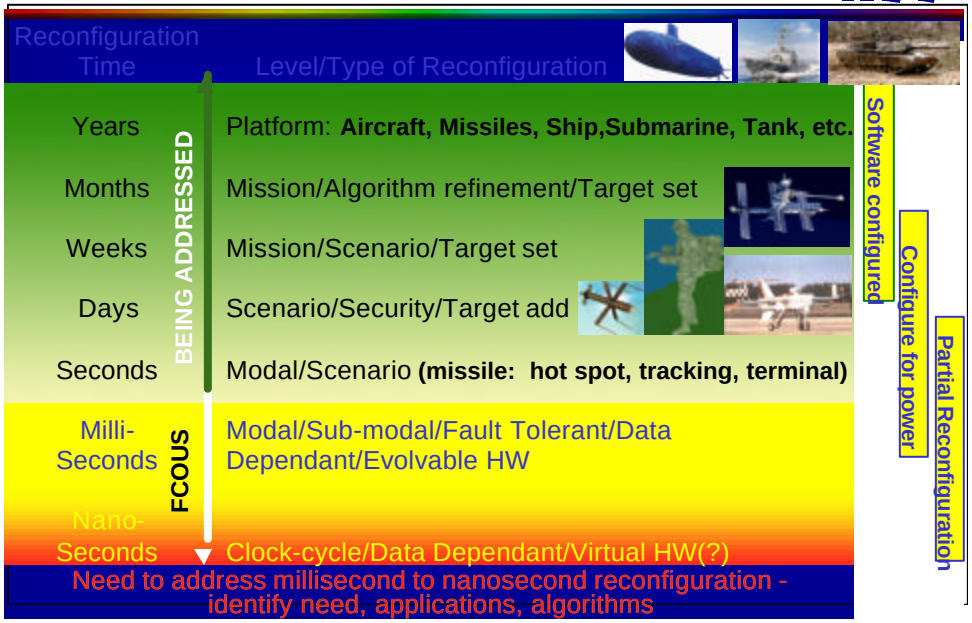
Tall Poles in the Tent



RECONFIGURATION



Dynamic Reconfiguration

- Need to address microsecond to nanosecond reconfiguration -
  - **identify need,**
  - **identify specific applications,**
  - **develop algorithms,**
  - **identify hardware platforms**
    - **exploit emulation where possible**
    - **exploit partial reconfiguration, even if limited**
  - **runtime system support**

Reconfiguration times are taking up greater than 75% of the total processing times!!!

DYNAMIC RECONFIGURATION

Three “flavors” of dynamic reconfiguration

- Constant Interconnect
  - the interconnect remains the same
  - function blocks are reconfigured to effect a new capability
- Constant Function
  - function blocks remain the same
  - interconnect is reconfigured to effect a new capability
- Complete Reconfiguration
  - both interconnect and function blocks change to effect a new capability

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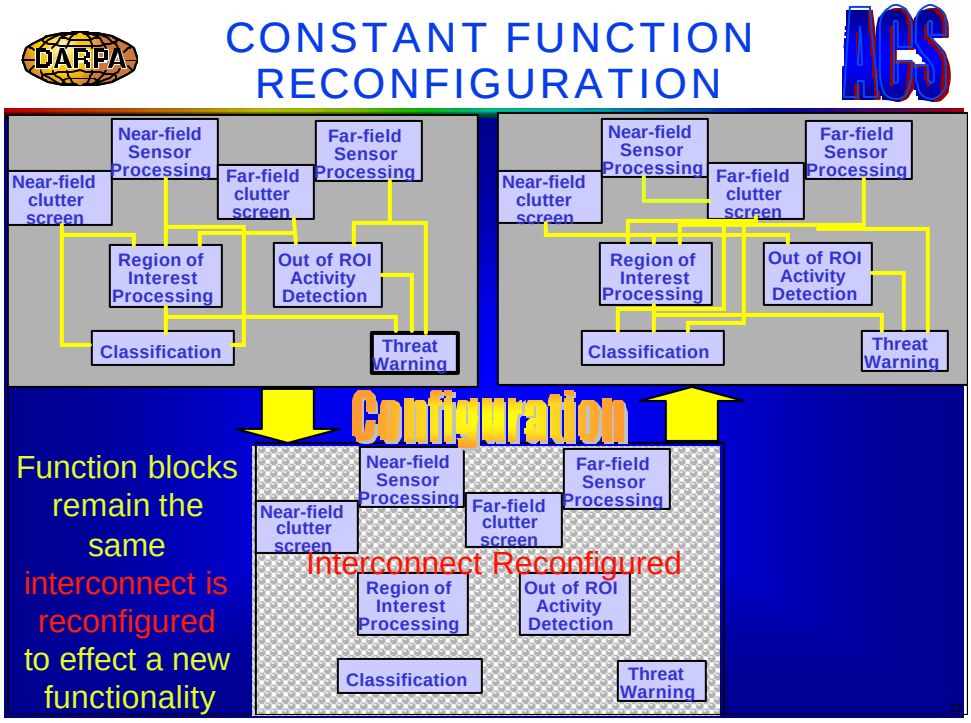

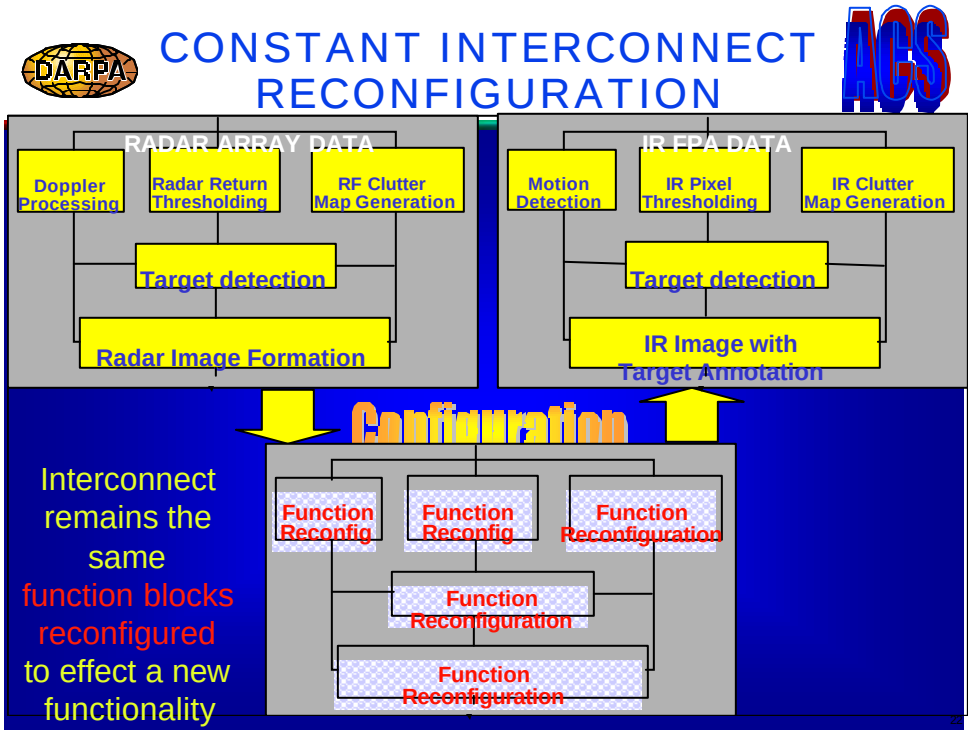

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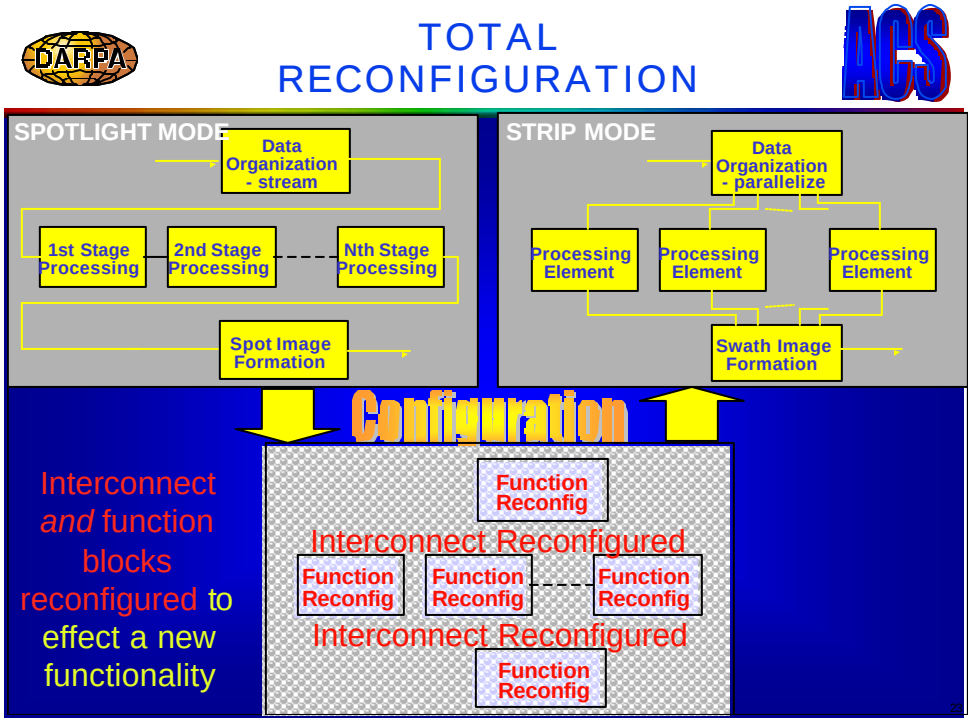

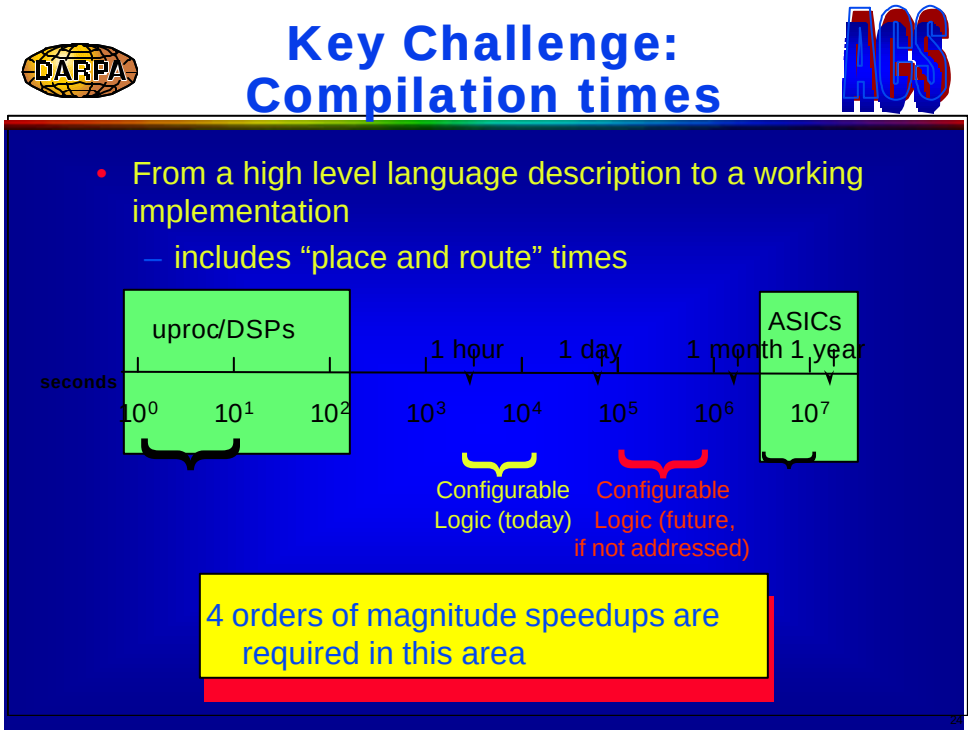

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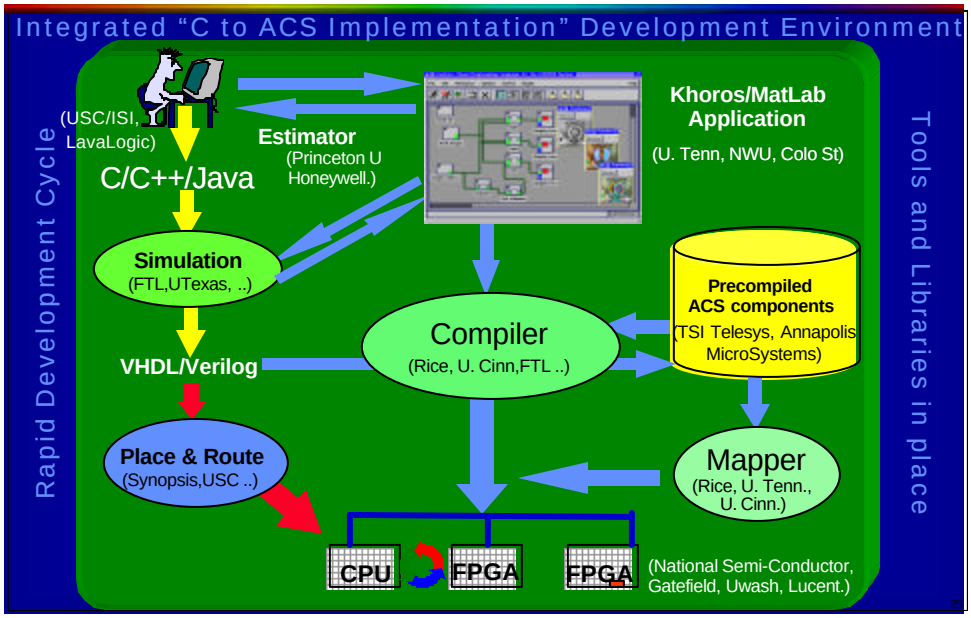
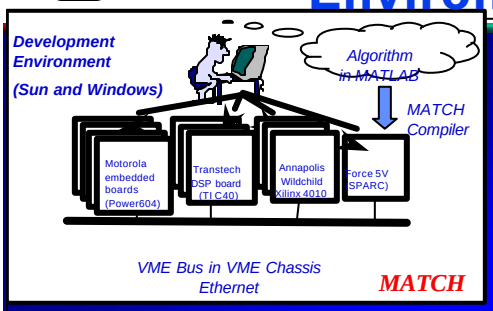
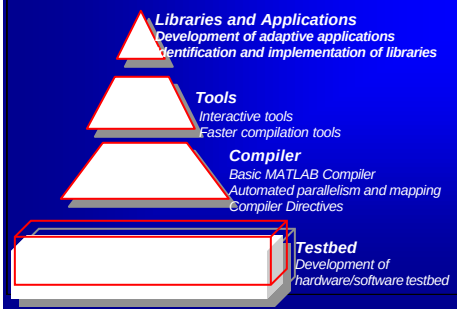
Things to Come



Match: ACS Development Environments





NEW IDEAS

- Integrated fully automated compiler
- Automatic parallelism detection/mapping
- Novel algorithms for fast compilation
- Tools for interactive evaluation
- Application driven (e.g. STAP/ATR)

IMPACT

- Reduce code development times from weeks to hours
- Compile high-level language (MATLAB programs) directly to embedded, DSP, and reconfigurable logic
- Efficient execution (within a factor of 2-4 of manual approach)
  - Satisfy throughput/latency constraints
  - Satisfy code size constraints
- 10-100X faster in compile times

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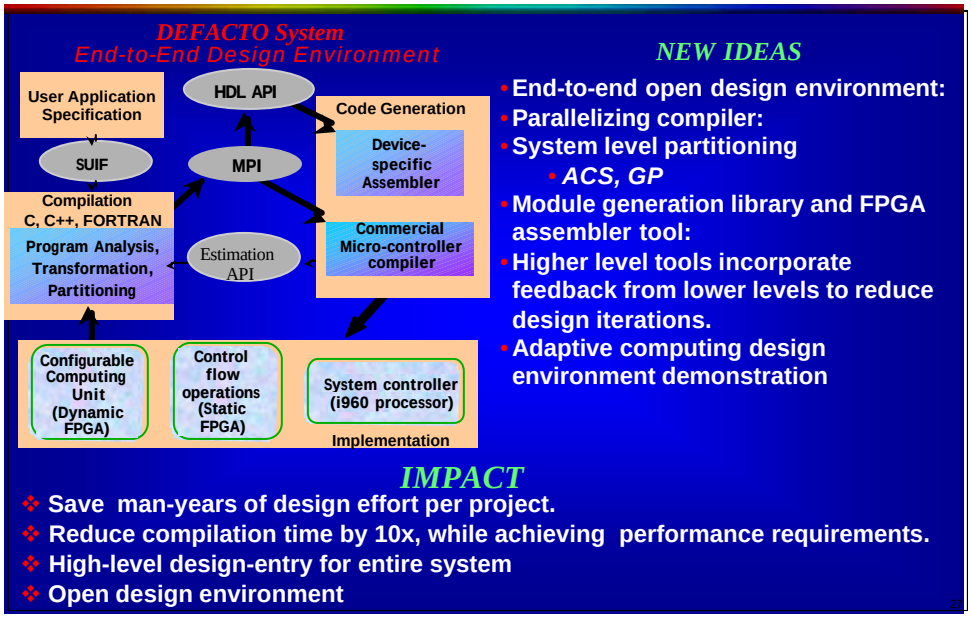
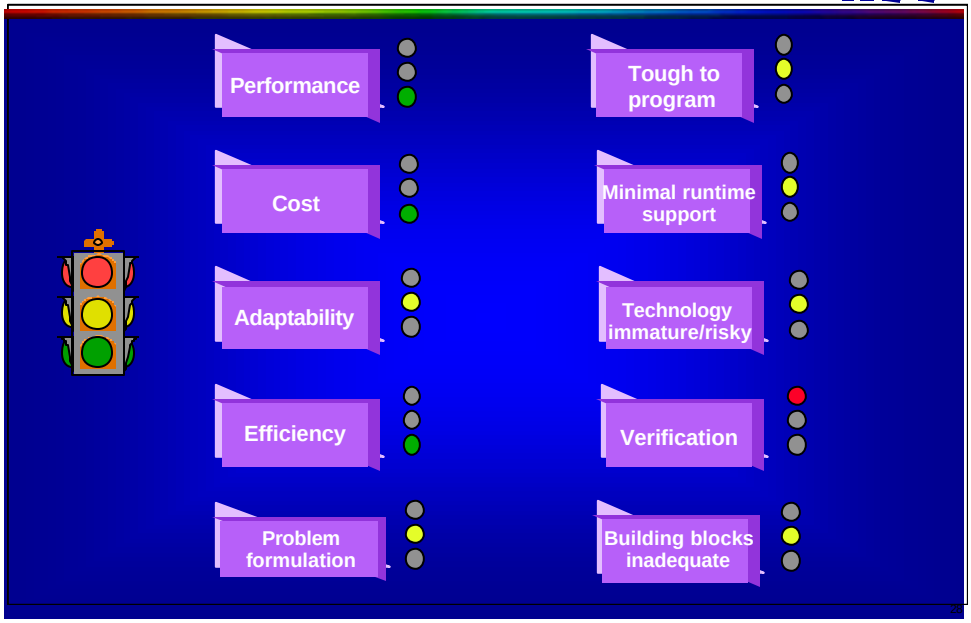
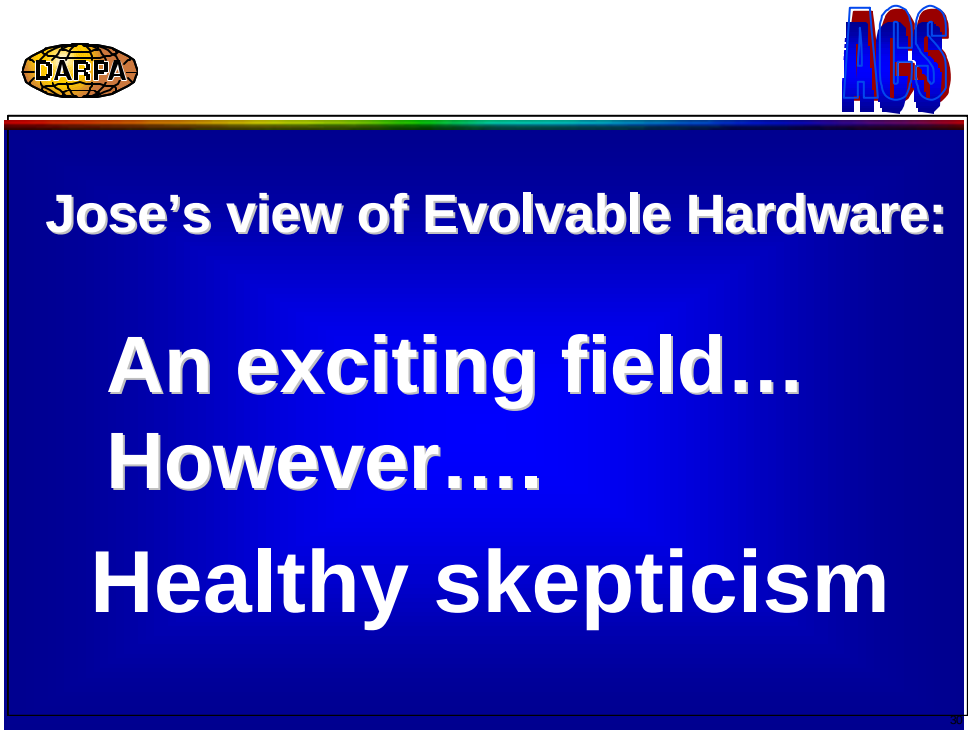
Defacto: ACS Development Environments



Summary




DARPA
ACS
ACS and Evolvable Hardware


DARPA
ACS
Jose's view of Evolvable Hardware:
An exciting field…
However….
Healthy skepticism

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Why ACS Interest?

- Using devices that are at the cornerstone of ACS
- Another way to explore the design space
- How to deal with increasing number of gates …
  - 1 Billion transistors = 400, 000, 000 gates
- A “solution” to the Place-Route problem
- IT’S FUN!!

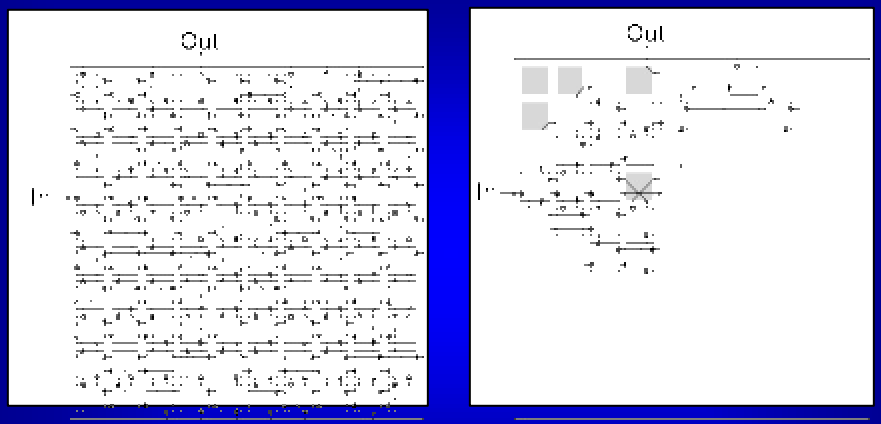
Evolvable Hardware ACS Interest

- What are the appropriate hardware building blocks to support exploitation of evolvable hardware?
  - Granularity
  - Digital/Analog?
  - Architecture
  - How/where to best conduct the fitness evaluation
- What user tools are required?
  - Front-end development environment
  - Debugging… how can we “see” what’s going on?
- What is the class of problems best /worst suited for Evol HW solutions?

Evolvable HW "Issues"

- **How to handle Verification?**
  - Safety: hardware and platform
- **Reproducibility**
  - Can the created circuit be readily reproduced, relocated, understood?
- **Robustness/Testability**

EH Solution for Freq Discriminator



Source: A. Thompson, U. Sussex

```
Freq: { 1KHz, 10KHz}
If Freq == 1KHz then
 set HIGH
else
 set LOW;
```

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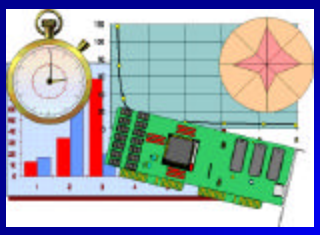
ACS Stressmarks



GOALS:

- Provide publicly available set of standard benchmarks for evaluating configurable computing systems
- Address the entire range of issues in benchmarking, including benchmark specification, procedures, metrics, and wide availability

How do we know we're "getting better"?

- **Versatility** - measures the ability to perform a varied computational sequence - *Image compression (2D Wavelet Transform, Quantization, Runlength Encoding, and Entrophy Encoding)*
- **Capacity** - measures the usable reconfigurable capacity - *Huffman Encoding*
- **Timing Sensitivity** - measures the ability to implement a time-critical application - *CORDIC Algorithm*
- **Scalability** - measures the ability to implement an application across multiple-devices - *Fast Fourier Transform (FFT)*
- **Interfacing** - measures the ability to operate within a heterogeneous architecture, interface to a general-purpose and/or application-specific processor - *Continuous False Alarm Rate*
- **CAD Benchmark** - measure the ability to utilize/support an architecture - *Boolean Satisfiability*

VECTOR, IMAGE, SIGNAL PROCESSING

GOALS:

- Create a *Vector/Signal/Image Processing* (VSIP) Forum composed of industry, government, users, and academia
- Define industry standard vector, signal, and image processing API/library for embedded real-time signal processing
- Enable standardization for software portability - reuse, interoperability, low cost COTS upgrade path, lower life cycle costs, *etc.*
- **Develop and freely distribute: API Standard Spec., C Reference Implementation, Test Suite**

STATUS:

- Draft VSIP Standards Documents available: ***Signal Processing, Vector, Image Processing, Support, Scalar, and Linear Algebra Library Routines*** (in .pdf Format via VSIP web site)
- Single Processor VSIP C Reference Library, Core Workstation Library, and Validation Suite (not all functions) in pre-Alpha/Alpha testing and evaluation
- Current VSIP Member organizations include Embedded Processing developers, Workstation developers, Tool developers, Academia, and Government

VSIP Site: http://www.vsip.org

VSIP Forum Chair: David Schwartz, HRL Laboratory, Malibu, CA
(310) 317-5216 daschwartz@hrl.com